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L5 AND directive	9

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L6

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DATE: Sunday, May 09, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=NO; OP=OR		
L6	L5 AND directive	9	L6
L5	(5724504 6112312 6484135 6370492 6557157 6708143 6102960 5452457 5530964 6115746 6343261 5598344 6523172 6475753 5394347 5522036 5604895 5918037 6182258 6347388 6675138 6691079 6292830 6416838 6421613 6618839 5452227 5805470 5815688 6074426 6415396 5680619 6198416 6216252 6216252 6288120 6691249 5761408 5339262 5353243 5625580 5629876 5640337 4590581 4891773 5325309 5671352 6083269 6188975 6199031).pn.	49	L5
L4	L3 AND (test ADJ (generation OR generator))	11	L4
L3	L2 AND directive	71	L3
L2	L1 AND debug	1652	L2
L1	717/$$$.ccls. OR 714/$$$.ccls.	26604	L1

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Search Results - Record(s) 1 through 11 of 11 returned.

☐ 1. Document ID: US 6643803 B1

L4: Entry 1 of 11 File: USPT Nov 4, 2003

US-PAT-NO: 6643803
DOCUMENT-IDENTIFIER: US 6643803 B1

TITLE: Emulation suspend mode with instruction jamming

DATE-ISSUED: November 4, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		
Matt; David R.	Missouri City	TX		

US-CL-CURRENT: 714/38; 714/29, 714/799

ABSTRACT:

Emulation and debug circuitry is provided that can be incorporated into a variety of digital systems. A stop mode of operation is provided in which an associated processor stops processing instructions in response to a debug event. A real-time mode of operation is provided in which the processor stops processing background instructions in response to a debug event, but in which high priority interrupts are still processed. While running or suspended, the emulation circuitry can jam an instruction into the instruction register of the processor to cause processor resources to be read or written on behalf of the emulation circuitry. An embodiment of a processor core is provided that is a programmable digital signal processor (DSP) with variable instruction length, offering both high code density and easy programming. Architecture and instruction set are optimized for low power consumption and high efficiency execution of DSP algorithms, such as for wireless telephones, as well as pure control tasks.

19 Claims, 22 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 13

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. De

☐ 2. Document ID: US 6567933 B1

L4: Entry 2 of 11 File: USPT May 20, 2003

US-PAT-NO: 6567933
DOCUMENT-IDENTIFIER: US 6567933 B1

TITLE: Emulation suspension mode with stop mode extension

DATE-ISSUED: May 20, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		
Matt; David R.	Missouri City	TX		

US-CL-CURRENT: 714/31; 710/59

ABSTRACT:

Emulation and debug circuitry is provided that can be incorporated into a variety of digital systems. A stop mode of operation is provided in which an associated processor stops processing instructions in response to a debug event. A real-time mode of operation is provided in which the processor stops processing background instructions in response to a debug event, but in which high priority interrupts are still processed. Interrupts are classified and processed accordingly when the processor is stopped by a debug event. While suspended for a debug event, a frame counter keeps track of interrupt debug state if multiple interrupts occur. While running or suspended, the emulation circuitry can jam an instruction into the instruction register of the processor to cause processor resources to be read or written on behalf of the emulation circuitry. Read/write transactions are qualified by an expected frame count to maintain correspondence between test host software and multiple debug/interrupt events. Architecture and instruction set are optimized for low power consumption and high efficiency execution of DSP algorithms, such as for wireless telephones, as well as pure control tasks.

19 Claims, 19 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 12

☐ 3. Document ID: US 6564339 B1

L4: Entry 3 of 11 File: USPT May 13, 2003

US-PAT-NO: 6564339
DOCUMENT-IDENTIFIER: US 6564339 B1

TITLE: Emulation suspension mode handling multiple stops and starts

DATE-ISSUED: May 13, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		
Matt; David R.	Missouri City	TX		

US-CL-CURRENT: 714/30; 714/25, 714/27, 714/28

ABSTRACT:

Emulation and debug circuitry is provided that can be incorporated into a variety of digital systems. A stop mode of operation is provided in which an associated processor stops processing instructions in response to a debug event. A real-time mode of operation is provided in which the processor stops processing background instructions in response to a debug event, but in which high priority interrupts are still processed. Interrupts are classified and processed accordingly when the processor is stopped by a debug event. While suspended for a debug event, a frame counter keeps track of interrupt debug state if multiple interrupts occur. While running or suspended, the emulation circuitry can jam an instruction into the instruction register of the processor to cause processor resources to be read or written on behalf of the emulation circuitry. Read/write transactions are qualified by an expected frame count to maintain correspondence between test host software and multiple debug/interrupt events. Architecture and instruction set are optimized for low power consumption and high efficiency execution of DSP algorithms, such as for wireless telephones, as well as pure control tasks.

17 Claims, 19 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 12

☐ 4. Document ID: US 6557116 B1

L4: Entry 4 of 11 File: USPT Apr 29, 2003

US-PAT-NO: 6557116
DOCUMENT-IDENTIFIER: US 6557116 B1

TITLE: Emulation suspension mode with frame controlled resource access

DATE-ISSUED: April 29, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		
Matt; David R.	Missouri City	TX		

US-CL-CURRENT: 714/28; 714/27, 714/30, 714/34

ABSTRACT:

Emulation and debug circuitry is provided that can be incorporated into a variety of digital systems. A stop mode of operation is provided in which an associated processor stops processing instructions in response to a debug event. A real-time

mode of operation is provided in which the processor stops processing background instructions in response to a debug event, but in which high priority interrupts are still processed. Interrupts are classified and processed accordingly when the processor is stopped by a debug event. While suspended for a debug event, a frame counter keeps track of interrupt debug state if multiple interrupts occur. While running or suspended, the emulation circuitry can jam an instruction into the instruction register of the processor to cause processor resources to be read or written on behalf of the emulation circuitry. Read/write transactions are qualified by an expected frame count to maintain correspondence between test host software and multiple debug/interrupt events. Architecture and instruction set are optimized for low power consumption and high efficiency execution of DSP algorithms, such as for wireless telephones, as well as pure control tasks.

11 Claims, 19 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 12

☐ 5. Document ID: US 6553513 B1

L4: Entry 5 of 11 File: USPT Apr 22, 2003

US-PAT-NO: 6553513
DOCUMENT-IDENTIFIER: US 6553513 B1

TITLE: Emulation suspend mode with differing response to differing classes of interrupts

DATE-ISSUED: April 22, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		
Matt; David R.	Missouri City	TX		

US-CL-CURRENT: 714/28; 714/25, 714/27, 714/30

ABSTRACT:

Emulation and debug circuitry is provided that can be incorporated into a variety of digital systems. A stop mode of operation is provided in which an associated processor stops processing instructions in response to a debug event. A real-time mode of operation is provided in which the processor stops processing background instructions in response to a debug event, but in which high priority interrupts are still processed. Interrupts are classified and processed accordingly when the processor is stopped by a debug event. While suspended for a debug event, a frame counter keeps track of interrupt debug state if multiple interrupts occur. While running or suspended, the emulation circuitry can jam an instruction into the instruction register of the processor to cause processor resources to be read or written on behalf of the emulation circuitry. Read/write transactions are qualified by an expected frame count to maintain correspondence between test host software and multiple debug/interrupt events. An embodiment of a processor core is provided that is a programmable digital signal processor (DSP) with variable instruction

length, offering both high code density and easy programming. Architecture and instruction set are optimized for low power consumption and high efficiency execution of DSP algorithms, such as for wireless telephones, as well as pure control tasks.

17 Claims, 34 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 21

☐ 6. Document ID: US 6463582 B1

L4: Entry 6 of 11 File: USPT Oct 8, 2002

US-PAT-NO: 6463582
DOCUMENT-IDENTIFIER: US 6463582 B1

TITLE: Dynamic optimizing object code translator for architecture emulation and dynamic optimizing object code translation method

DATE-ISSUED: October 8, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lethin; Richard A.	New York	NY		
Bank, III; Joseph A.	New York	NY		
Garrett; Charles D.	Seattle	WA		
Wada; Mikayo	Kawasaki			JP
Sakurai; Mitsuo	Kawasaki			JP

US-CL-CURRENT: 717/158; 717/138, 717/139

ABSTRACT:

An optimizing object code translation system and method perform dynamic compilation and translation of a target object code on a source operating system while performing optimization. Compilation and optimization of the target code is dynamically executed in real time. A compiler performs analysis and optimizations that improve emulation relative to template-based translation and interpretation such that a host processor which processes larger order instructions, such as 32-bit instructions, may emulate a target processor which processes smaller order instructions, such as 16-bit and 8-bit instructions. The optimizing object code translator does not require knowledge of a static program flow graph or memory locations of target instructions prior to run time. In addition, the optimizing object code translator does not require knowledge of the location of all join points into the target object code prior to execution. During program execution, a translator records branch operations. The logging of information identifies instructions and instruction join points. When a number of times a branch operation is executed exceeds a threshold, the destination of the branch becomes a seed for compilation and code portions between seeds are defined as segments. A segment may be incomplete allowing for modification or replacement to account for a new flow of program control during real time program execution.

32 Claims, 37 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 19

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 7. Document ID: US 6081885 A

L4: Entry 7 of 11 File: USPT Jun 27, 2000

US-PAT-NO: 6081885
DOCUMENT-IDENTIFIER: US 6081885 A

TITLE: Method and apparatus for halting a processor and providing state visibility on a pipeline phase basis

DATE-ISSUED: June 27, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Deao; Douglas E.	Brookshire	TX		
Seshan; Natarajan	Houston	TX		

US-CL-CURRENT: 712/227; 712/220, 714/13, 714/16

ABSTRACT:

A data processing system on an integrated circuit 42 with microprocessor 1 and peripheral devices 60-61 is provided with an emulation unit 50 which allows debugging and emulation of integrated circuit 42 when connected to an external test system 51. Microprocessor 1 has in instruction execution pipeline that has several execution phases which involve fetch/decode units 10a-c and functional execution units 12, 14, 16 and 18. The pipeline of microprocessor 1 is unprotected so that memory access latency to data memory 22 and register file 20 can be utilized by system program code which is stored in instruction memory 23. Emulation unit 50 provides means for emulating the unprotected pipeline of microprocessor 1 and for rapidly uploading and downloading memories 22-23. Microprocessor 1 is operable to halt in response to an emulation event with partially completed instructions still in the execution pipeline. Thus, emulation unit 50 can provide visibility to the state of the microprocessor on a single pipeline phase basis. Emulation unit 50 operates in a manner to prevent extraneous operations from occurring that could otherwise affect memories 22-23 or peripheral devices 60-61 during emulation.

15 Claims, 69 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 32

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☑ 8. Document ID: US 6065106 A

L4: Entry 8 of 11 File: USPT May 16, 2000

US-PAT-NO: 6065106
DOCUMENT-IDENTIFIER: US 6065106 A

TITLE: Resuming normal execution by restoring without refetching instructions in multi-word instruction register interrupted by debug instructions loading and processing

DATE-ISSUED: May 16, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Deao; Douglas E.	Brookshire	TX		
Seshan; Natarajan	Houston	TX		

US-CL-CURRENT: 712/24; 712/227, 714/30

ABSTRACT:

A data processing system on an integrated circuit 42 with microprocessor 1 and peripheral devices 60-61 is provided with an emulation unit 50 which allows debugging and emulation of integrated circuit 42 when connected to an external test system 51. Microprocessor 1 has in instruction execution pipeline which has several execution phases which involve fetch/decode units 10a-c and functional execution units 12, 14, 16 and 18. The pipeline of microprocessor 1 is unprotected so that memory access latency to data memory 22 and register file 20 can be utilized by system program code which is stored in instruction memory 23. Emulation unit 50 provides means for emulating the unprotected pipeline of microprocessor 1 and for rapidly uploading and downloading memories 22-23. During emulation, the fetching of instructions from program memory can be halted. A packet of instructions can be transferred from the emulation unit to the instruction register of the processor via a test port and executed without fetching instructions from instruction memory. The packet of instructions can perform various tasks, such as loading or storing data or loading new instructions into program memory. Emulation unit 50 operates in a manner to prevent extraneous operations from occurring which could otherwise affect memories 22-23 or peripheral devices 60-61 during emulation.

22 Claims, 69 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 33

☐ 9. Document ID: US 6055649 A

L4: Entry 9 of 11 File: USPT Apr 25, 2000

US-PAT-NO: 6055649
DOCUMENT-IDENTIFIER: US 6055649 A

TITLE: Processor test port with scan chains and data streaming

DATE-ISSUED: April 25, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Deao; Douglas E.	Brookshire	TX		
Seshan; Natarajan	Houston	TX		
Lell; Anthony J.	Houston	TX		

US-CL-CURRENT: 714/30

ABSTRACT:

A data processing system on an integrated circuit 42 with microprocessor 1 and peripheral devices 60-61 is provided with an emulation unit 50 which allows debugging and emulation of integrated circuit 42 when connected to an external test system 51. Microprocessor 1 has in instruction execution pipeline which has several execution phases which involve fetch/decode units 10a-c and functional execution units 12, 14, 16 and 18. The pipeline of microprocessor 1 is unprotected so that memory access latency to data memory 22 and register file 20 can be utilized by system program code which is stored in instruction memory 23. Emulation unit 50 provides means for emulating the unprotected pipeline of microprocessor 1 and for rapidly uploading and downloading memories 22-23. Emulation unit 50 operates in a manner to prevent extraneous operations from occurring which could otherwise affect memories 22-23 or peripheral devices 60-61 during emulation.

20 Claims, 69 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 32

☑ 10. Document ID: US 6016555 A

L4: Entry 10 of 11 File: USPT Jan 18, 2000

US-PAT-NO: 6016555
DOCUMENT-IDENTIFIER: US 6016555 A

TITLE: Non-intrusive software breakpoints in a processor instruction execution pipeline

DATE-ISSUED: January 18, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Deao; Douglas E.	Brookshire	TX		
Seshan; Natarajan	Houston	TX		

US-CL-CURRENT: 714/35; 714/34

ABSTRACT:

A data processing system on an integrated circuit 42 with microprocessor 1 and peripheral devices 60-61 is provided with an emulation unit 50 which allows debugging and emulation of integrated circuit 42 when connected to an external test system 51. Microprocessor 1 has in instruction execution pipeline which has several execution phases which involve fetch/decode units 10a-c and functional execution units 12, 14, 16 and 18. The pipeline of microprocessor 1 is unprotected so that memory access latency to data memory 22 and register file 20 can be utilized by system program code which is stored in instruction memory 23. Emulation unit 50 provides means for emulating the unprotected pipeline of microprocessor 1 and for rapidly uploading and downloading memories 22-23. Emulation unit 50 operates in a manner to prevent extraneous operations from occurring which could otherwise affect memories 22-23 or peripheral devices 60-61 during emulation.

20 Claims, 69 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 32

☑ 11. Document ID: US 5828824 A

L4: Entry 11 of 11 File: USPT Oct 27, 1998

US-PAT-NO: 5828824
DOCUMENT-IDENTIFIER: US 5828824 A

TITLE: Method for debugging an integrated circuit using extended operating modes

DATE-ISSUED: October 27, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		

US-CL-CURRENT: 714/25; 714/30, 714/38, 714/46, 714/733

ABSTRACT:

A method of testing an integrated circuit 104 which may have multiple modules 204a-d is provided. Target interface 200 provides an interface for connecting target system 104 to a test system which is an extension of IEEE 1149.1. Target system 104 may have multiple devices 202, each having multiple modules 204. Each device 202 has device interface 210 which connects to target interface 200. Decoder 1020 decodes certain signals from interface 200 to enable Extended Operating Modes which allow test codes to be easily directed to any one of modules 204a-d. Hardware and software debugging of system 104 is aided by interface 200 and production testing of system 104 is simplified.

7 Claims, 15 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 9

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Terms	Documents
L3 AND (test ADJ (generation OR generator))	11

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